1. A method of forming a semiconductor memory structure comprising:

forming a capacitor support structure over a digit line and over a substrate, said support structure including interconnected sidewalls defining containers between said sidewalls, at least some of said containers being formed over respective capacitor plugs; and

forming capacitors in at least some of said containers.

2. The method according to claim 1 wherein said capacitor plugs extend to a transistor region formed in said substrate.

3. The method according to claim 1 wherein said support structure comprises a single layer of material.

4. The method according to claim 1 wherein said support structure comprises a plurality of layers of material.

5. The method according to claim 1 further comprising forming said support structure by etching at least one layer of the support structure forming material to form one of rectangular, oval, and square alternating block pattern.

6. The method according to claim 5 further comprising forming sidewall spacers on vertical surfaces of said block pattern.

7. The method according to claim 5 further comprising transferring said block pattern into an underlying layer of said support structure forming material.

8. The method according to claim 7 further comprising forming sidewall spacers on sidewalls of said transferred block pattern.

9. The method according to claim 8 further comprising forming said capacitor support structure from said sidewall spacers.

10. The method according to claim 5 further comprising forming a metal layer on top of said alternating block pattern.

11. The method according to claim 10 wherein said metal layer consists of one of titanium, palladium, and tungsten.

12. The method according to claim 10 further comprising annealing said metal layer to form a silicide.

13. The method according to claim 5 wherein said support structure forming material comprises a BPSG layer between a nitride layer and a polysilicon layer.

14. The method according to claim 5 wherein said support structure forming material comprises a nitride layer beneath a BPSG layer, a polysilicon layer over said BPSG layer, and a TEOS layer over said polysilicon layer.

15. The method according to claim 5 wherein said support structure forming material comprises a nitride layer beneath a BPSG or PSG layer, a polysilicon layer over said BPSG layer, and a TEOS layer over said polysilicon layer.

16. The method according to claim 8 wherein said sidewall spacers comprise polysilicon spacers.

17. The method according to claim 8 wherein said sidewall spacers comprise titanium nitride spacers.

18. The method according to claim 8 wherein said sidewall spacers comprise TEOS spacers that are etched from between the capacitors.

19. The method according to claim 8 wherein said sidewall spacers comprise platinum spacers.

20. The method according to claim 8 wherein said sidewall spacers comprise amorphous silicon spacers.

21. The method according to claim 20 further comprising seeding and annealing said spacers to form an HSG layer.

22. The method according to claim 1 wherein said capacitors are formed as metal insulator metal capacitors.

23. The method according to claim 22 wherein said capacitors comprise a first platinum layer, a Ta_2O_5 or BST layer, and a second platinum layer.

24. The method according to claim 23 further comprising forming a conductive barrier layer beneath either the first or second platinum layer.

25. The method according to claim 24 wherein said conductive barrier layer comprises tantalum nitride or tantalum silicon nitride.

26. The method according to claim 1 wherein said capacitors are formed as metal insulator silicon capacitors.

27. The method according to claim 26 wherein said capacitors comprise an HSG layer, a Ta_2O_5 layer, and a titanium nitride layer.

28. The method according to claim 8 wherein said spacers are electrically connected to a cell plate and function as part of the cell plate of the capacitor.

29. A method of forming a capacitor array comprising:

forming a digit line over a substrate, providing electrical contacts extending above said digit line, forming a pattern of interconnected sidewalls over said electrical contacts, and forming capacitors electrically connected to said electrical contacts in containers defined by said sidewalls.

30. The method according to claim 29 wherein said electrical contacts extend to a transistor region formed in said substrate.

31. The method according to claim 29 further comprising forming said interconnected sidewalls in a support structure.

32. The method according to claim 31 wherein said support structure comprises a single layer of material.

33. The method according to claim 31 wherein said support structure comprises a plurality of layers of material.

34. The method according to claim 31 further comprising forming an alternating block pattern in at least one layer of material in said support structure.

35. The method according to claim 34 further comprising forming sidewall spacers on vertical surfaces of said block pattern.

36. The method according to claim 34 further comprising transferring said block pattern into an underlying layer of said support structure.

37. The method according to claim 36 further comprising forming sidewall spacers on said transferred block pattern.

38. The method according to claim 37 further comprising forming said interconnected sidewalls from said sidewall spacers.

39. The method according to claim 34 further comprising forming a metal layer on top of said alternating block pattern.

40. The method according to claim 39 wherein said metal layer consists of one of titanium, palladium, and tungsten.

41. The method according to claim 33 further comprising annealing said metal layer to form a silicide.

42. The method according to claim 33 wherein said plurality of layers comprises a BPSG layer between a nitride layer and a polysilicon layer.

43. The method according to claim 33 wherein said plurality of layers comprises a nitride layer beneath a BPSG layer, a polysilicon layer over said BPSG layer, and a TEOS layer over said polysilicon layer.

44. (Amended) The method according to claim 33 wherein said plurality of layers comprises a nitride layer beneath a PSG layer, a polysilicon layer over said PSG layer, and a TEOS layer over said polysilicon layer.

45. The method according to claim 37 wherein said sidewall spacers comprise polysilicon spacers.

46. The method according to claim 37 wherein said sidewall spacers comprise titanium nitride spacers.

47. The method according to claim 37 wherein said sidewall spacers comprise TEOS spacers that are etched from between the capacitors.

48. The method according to claim 37 wherein said sidewall spacers comprise platinum spacers.

49. The method according to claim 37 wherein said sidewall spacers comprise amorphous silicon spacers.

50. The method according to claim 43 further comprising seeding and annealing said spacers to form an HSG layer.

51. The method according to claim 29 wherein said capacitors are formed as metal insulator metal capacitors.

52. The method according to claim 51 wherein said capacitors comprise a first platinum layer, a Ta_2O_5 or BST layer, and a second platinum layer.

53. The method according to claim 52 further comprising forming a conductive barrier layer beneath either the first or second platinum layer.

54. The method according to claim 53 wherein said conductive barrier layer comprises tantalum nitride or tantalum silicon nitride.

55. The method according to claim 29 wherein said capacitors are formed as metal insulator silicon capacitors.

56. The method according to claim 55 wherein said capacitors comprise an HSG layer, a Ta_2O_5 layer, and a titanium nitride layer.

57. The method according to claim 37 wherein said spacers are electrically connected to a cell plate and function as part of the cell plate of the capacitor.

58. A method of forming integrated circuitry comprising:

providing a transistor array over a substrate;

providing a digit line over said transistor array;

providing a plurality of layers of material over said digit line;

forming one of square, rectangular, and oval pattern in at least one of said plurality of layers of material, said pattern being defined by having raised structures alternating with recesses;

transferring said pattern into an underlying layer in said plurality of layers;

forming sidewall spacers on vertical surfaces of said transferred pattern; and

forming a capacitor container array defined by said sidewall spacers.

59. The method according to claim 58 further comprising forming capacitors in said containers.

60. The method according to claim 58 further comprising forming cell node polysilicon plugs extending above said digit line.

61. The method according to claim 58 further comprising etching only the top layer of said plurality of layers of material to from said pattern.

62. The method according to claim 58 further comprising etching two or more of said plurality of layers of material to form said pattern.

63. The method according to claim 58 further comprising forming a metal layer on top of said pattern.

64. The method according to claim 63 wherein said metal layer consists of one of titanium, palladium, and tungsten.

65. The method according to claim 63 further comprising annealing said metal layer to form a silicide.

66. The method according to claim 58 wherein said plurality of layers of material comprises a BPSG layer between a polysilicon layer and a nitride layer.

67. The method according to claim 58 wherein said plurality of layers of material comprises a nitride layer beneath a BPSG layer, a polysilicon layer over said BPSG layer, and a TEOS layer over said polysilicon layer.

68. The method according to claim 58 wherein said plurality of layers of material comprises a nitride layer beneath one of a PSG and a BPSG layer, a polysilicon layer over said one of BPSG and PSG layer, and a TEOS layer over said polysilicon layer.

69. The method according to claim 58 wherein said sidewall spacers comprise polysilicon spacers.

70. The method according to claim 58 wherein said sidewall spacers comprise titanium nitride spacers.

71. The method according to claim 58 wherein said sidewall spacers comprise TEOS spacers that are etched from between the capacitors.

72. The method according to claim 58 wherein said sidewall spacers comprise platinum spacers.

73. The method according to claim 58 wherein said sidewall spacers comprise amorphous silicon spacers.

74. The method according to claim 73 further comprising seeding and annealing said spacers to form an HSG layer.

75. The method according to claim 58 wherein said capacitors are formed as metal insulator metal capacitors.

76. The method according to claim 75 wherein said capacitors comprise a first platinum layer, a Ta_2O_5 or BST layer, and a second platinum layer.

77. The method according to claim 76 further comprising forming a conductive barrier layer beneath either the first or second platinum layer.

78. The method according to claim 77 wherein said conductive barrier layer comprises tantalum nitride or tantalum silicon nitride.

79. The method according to claim 58 wherein said capacitors are formed as metal insulator silicon capacitors.

80. The method according to claim 79 wherein said capacitors comprise an HSG layer, a Ta_2O_5 layer, and a titanium nitride layer.

81. The method according to claim 58 wherein said spacers are electrically connected to a cell plate and function as part of the cell plate of the capacitor.

82. An integrated circuit comprising:

a substrate;

a digit line over said substrate;

an array of interconnected sidewalls over said digit line, said interconnected sidewalls defining capacitor formation regions, and

a plurality of capacitors respectively formed in at least some of said capacitor formation regions.

83. The circuit according to claim 82 wherein said sidewalls comprise polysilicon sidewalls.

84. The circuit according to claim 82 wherein said sidewalls comprise titanium nitride sidewalls.

85. The circuit according to claim 82 wherein said sidewalls comprise platinum spacers.

86. The circuit according to claim 82 wherein said sidewalls comprise TEOS sidewalls that are etched from between the capacitors.

87. The circuit according to claim 82 wherein said capacitors are comprised of a nitride layer deposited between an HSG layer and another electrode layer.

88. The circuit according to claim 82 wherein said sidewalls comprise amorphous silicon sidewalls.

89. The circuit according to claim 88 further comprising seeding and annealing said sidewalls to form an HSG layer.

90. The circuit according to claim 82 wherein said capacitors are formed as metal insulator metal capacitors.

91. The circuit according to claim 90 wherein said capacitors comprise a first platinum layer, a Ta_2O_5 or BST layer, and a second platinum layer.

92. The circuit according to claim 91 further comprising forming a conductive barrier layer beneath either the first or second platinum layer.

93. The circuit to claim 92 wherein said conductive barrier layer comprises tantalum nitride or tantalum silicon nitride.

94. The circuit according to claim 82 wherein said capacitors are formed as metal insulator silicon capacitors.

95. The circuit according to claim 94 wherein said capacitors comprise an HSG layer, a Ta_2O_5 layer, and a titanium nitride layer.

96. The circuit according to claim 8 wherein said sidewalls are electrically connected to a cell plate and function as part of the cell plate of the capacitor.

97. A computer system comprising:

a processor; and

a memory device comprising an array of interconnected sidewalls over a digit line, said interconnected sidewalls defining capacitor formation regions, and a plurality of capacitors respectively formed in at least some of said capacitor formation regions.

98. The system according to claim 97 wherein said sidewalls comprise polysilicon sidewalls.

99. The system according to claim 97 wherein said sidewalls comprise platinum sidewalls.

100. The system according to claim 97 wherein said sidewalls comprise titanium nitride sidewalls.

101. The system according to claim 97 wherein said sidewalls comprise TEOS sidewalls that are etched from between the capacitors.

102. The system according to claim 97 wherein said capacitors are comprised of a nitride layer deposited between an HSG layer and another electrode layer.

103. The system according to claim 97 wherein said sidewalls comprise amorphous silicon sidewalls.

104. The system according to claim 97 wherein said sidewalls comprise HSG sidewalls.

105. The system according to claim 97 wherein said capacitors are formed as metal insulator metal capacitors.

106. The system according to claim 105 wherein said capacitors comprise a first platinum layer, a Ta_2O_5 or BST layer, and a second platinum layer.

107. The system according to claim 106 further comprising forming a conductive barrier layer beneath either the first or second platinum layer.

108. The system according to claim 107 wherein said conductive barrier layer comprises tantalum nitride or tantalum silicon nitride.

109. The system according to claim 97 wherein said capacitors are formed as metal insulator silicon capacitors.

110. The system according to claim 109 wherein said capacitors comprise an HSG layer, a Ta_2O_5 layer, and a titanium nitride layer.

111. The system according to claim 97 wherein said sidewalls are electrically connected to a cell plate and function as part of the cell plate of the capacitors.

112. The method according to claim 6 wherein said sidewall spacers comprise TEOS spacers and are left between said capacitors.

113. The method according to claim 37 wherein said sidewall spacers comprise TEOS spacers and are left between said capacitors.

114. The method according to claim 58 wherein said sidewall spacers comprise TEOS spacers and are left between said capacitors.

115. The circuit according to claim 82 wherein said sidewalls comprise TEOS sidewalls which are left between said capacitors.

116. The system according to claim 97 wherein said sidewalls comprise TEOS sidewalls which are left between said capacitors.